

**IN THE CLAIMS:**

A detailed listing of all claims that are, or were, in the application follows:

1 - 15 (cancelled).

16. (previously presented): A display element having internal optical output control circuitry, comprising:

at least one optical element integrated within a display element configured for displaying multiple optical states;

an input configured for receiving an array position addressing signal containing array position clocking and data which are delivered in common to all said display elements within a single or multidimensional display array;

a counter configured for maintaining an array position count in response to detecting said array position clocking from said input;

a memory configured for retaining an array position;

a comparison circuit configured for generating a data load signal in response to detecting a desired relationship between said array position maintained by said counter and said array position retained in said memory;

a latch circuit configured for loading data from said input in response to receipt of said data load signal; and

a driver circuit configured for outputting said data to update the optical state of said at least one optical element.

17. (currently amended): A display element as recited in claim 16, wherein said input comprises a single signal line coupled directly ~~directed~~ to each said display element within a given display array, or a signal superimposed on the power being supplied to each said display element within said given display array.

18. (previously presented): A display element as recited in claim 16, further comprising:

a shift register coupled to said input and configured to receive data bits of said array position addressing signal in response to said data load signal;

wherein said shift register is configured to output, in parallel, the data bits it has received to said latch.

19. (previously presented): A display element as recited in claim 16, wherein said memory comprises a non-volatile memory.

20. (currently amended): A display element as recited in claim 19, wherein said memory is configured for being loaded with an ~~[[a]]~~ array position value in response to a position programming operation.

21. (previously presented): A display element as recited in claim 16, wherein said input comprises a separate signal connection aside from the power and ground connections of said display element.

22. (previously presented): A display element as recited in claim 16, wherein said input is received as a signal superimposed over said power and ground connections to said display element.

23. (previously presented): A display element as recited in claim 16, wherein said array position clocking and data are received for each array address in each cycle of an array position addressing signal.

24. (previously presented): A display element as recited in claim 23, wherein said driver is configured for outputting said data to said at least one optical element in response to detecting the end of said cycle of said array position addressing signal.

25. (previously presented): A display element as recited in claim 16, wherein said driver circuit is configured for modulating the optical state of each of said optical elements to either an on or off state in response to said data from said latch circuit.

26. (currently amended): A display element as recited in claim 16, wherein said driver circuit is configured for modulating the optical state of each of said optical elements to a desired intensity, ~~and/or color,~~ or combination of intensity and color, in response to said data from said latch circuit.

27 - 46. (cancelled).

47. (previously presented): A display element having internal control circuitry, comprising:

at least one optical element integrated within a display element configured for displaying multiple optical states;

a memory configured for programming to a first address associated with the position of said display element within an array of said display elements;

means for extracting output data from a data signal, received in parallel by the display element and other display elements within an array of display elements, in response to matching a second address received on said data signal with said first address; and

means for modulating the output of said at least one optical element in response to said extracted output data.

48. (previously presented): A display element as recited in claim 47, wherein said first address comprises at least one axis of addressing.

49. (previously presented): A display element as recited in claim 48, wherein said first address comprises a row and column address.

50. (previously presented): A display element as recited in claim 47, wherein said means for extracting data is configured for extracting a predetermined number of data

bits from said data signal.

51. (previously presented): A display element as recited in claim 50, wherein said means for extracting data is configured for counting clocks on said data signal for determining said second address.

52. (previously presented): A display element as recited in claim 51, wherein said clocks comprise column and row clocks.

53 (previously presented): A display element as recited in claim 51, wherein said means for extracting data is configured for detecting a reset clock to reset the clocks being counted in determining said second address.

54. (currently amended): A display element as recited in claim 47, wherein said data signal signal comprises either a single signal line coupled directly ~~directed~~ to each said display element within a given array of said display elements, or is superimposed on the power being supplied to each said display element within the array of display elements.

55. (previously presented): A display element as recited in claim 47, wherein said means for modulating the output of the optical state of said at least one optical element is configured to update the optical state of said optical element at a fixed position within cycles of said data signal.

56. (previously presented): A display element as recited in claim 55, wherein said fixed position occurs at the end of a cycle of said data signal.

57. (previously presented): A display element as recited in claim 47, wherein said means for extracting data from said common array positioning addressing signal, comprises:

- a counter configured for counting clocks to determine said second address within said data signal;

- an address comparator for generating a matching signal in response to detecting a predetermined relationship between said second address determined by said counter and said first address retained within said memory; and

- a data store configured for collecting data bits from said data signal in response to said matching signal.

58. (currently amended): A display element as recited in claim 47, wherein said modulating means comprises:

- a latch configured for latching and outputting data bits from said data store; and
- a driver circuit configured for driving said at least one optical element to provide intensity, ~~and/or color,~~ or combination of intensity and color, control in response to output data being output from said latch.

59. (previously presented): A display element as recited in claim 58, wherein said latch is configured to output the received data in response to a predetermined position within each cycle of the data signal.

60. (previously presented): A display element as recited in claim 47, wherein said optical element comprises one light emitting diode (LED) of a desired color, or multiple LEDs of at least one color.

61. (previously presented): A display element having internal control circuitry, comprising:

at least one optical element integrated within a display element configured for displaying multiple optical states;

a memory configured for storing a first address for the display element;

means for extracting output control data from a data signal, received in parallel with other display elements within an array of the display elements, in response to matching a second address received from the data signal with said first address; and

means for modulating the output state of at least one said optical element in response to said extracted output control data.

62. (previously presented): A display element as recited in claim 61, further comprising means for programming said memory to said first address in response to the position of the display element within an array of the display elements.

63. (previously presented): A display element as recited in claim 62, wherein said programming means is configured for loading said second address from the data signal in response to a programming signal received by said display element and not by other display elements within an array which are not to respond to given said second address.

64. (previously presented): A display element as recited in claim 63, wherein said programming means is configured to program said second address in response to a combination of data received from said data signal and said programming signal.

65. (previously presented): A display element as recited in claim 63, further comprising an optical detector within said display element, said optical detector configured for receiving said programming signal.

66. (previously presented): A display element as recited in claim 65, wherein said optical detector comprises one or more of said at least one optical elements which are configured for both displaying optical states and detecting optical input.

67. (previously presented): A display element as recited in claim 66, wherein said optical detector comprises at least one separate optical input sensor integrated within said display element.



68. (previously presented): A display element as recited in claim 61, wherein said output control data is received on the data signal in a sequential scan form or random form.

69. (previously presented): A display element having internal control circuitry, comprising:

at least one optical element integrated within a display element configured for displaying multiple optical states;

a memory configured for storing a first address for the display element in response to the position of the display element containing said at least one optical element within an array of said display elements;

means for extracting output control data from a common data signal received in parallel with other display elements within an array of the data elements, said output control data being extracted in response to detecting a desired relationship between said first address stored in memory and a second address received over said common data signal; and

means for modulating the output of at least one said optical element in response to said extracted output control data.

70. (previously presented): A display element having internal control circuitry, comprising:

at least one optical element integrated within a display element configured for displaying multiple optical states;

means for outputting optical state data, received from a data signal, to said at least one optical element in response to matching a first address received from the data signal with a second address programmed within said means to the position of the display element within an array of the display elements.

71. (previously presented): A display element as recited in claim 70, wherein said outputting means is configured for programming said second address in-situ.

72. (previously presented): A display element as recited in claim 70, wherein said outputting means is configured for receiving said data signal in parallel with other display elements within the array of display elements.

73. (previously presented): A display element as recited in claim 70, wherein said second address is programmed into non-volatile memory within said outputting means.

74 - 76. (cancelled).

77. (new): A display element as recited in claim 47, wherein said display element is contained within an optical housing configured with a transparent portion through which the state of said at least one optical element can be viewed.

78. (new): A display element as recited in claim 47, wherein said memory is configured for storing said first address for the display element in response to a

programming operation that programs the position of said display element according to its position within an array of display elements.

79. (new): A display element as recited in claim 78, wherein said programming operation is performed in response to receiving an external programming signal while said display element is in a programming mode which loads an address received in parallel by the display element as said first address into said memory.

80. (new): A display element as recited in claim 79, wherein said external programming signal comprises an optical signal.

81. (new): A display element as recited in claim 47, wherein at least the portion of said memory configured for programming to a first address comprises a non-volatile memory.

82. (new): A display element as recited in claim 58, wherein said driver circuit is configured for providing analog or digital intensity control.

83. (new): A display element as recited in claim 47, wherein said optical element, said memory, said extracting means and said modulating means are contained on, or coupled to, the same integrated circuit die.

84. (new): A display element as recited in claim 47, wherein said optical element, said memory, said extracting means and said modulating means are contained on at least two integrated circuit die which are coupled to one another and retained in said optical housing.